What is claimed is:

1. A method for creation of an interconnect pattern, comprising:

providing a layer of conductive material over a semiconductor surface, a layer of Anti Reflective Coating (ARC) having been deposited over the layer of conductive material;

depositing a layer of Photo-Active Dielectric (PAD) over the layer of ARC;

patterning and developing the layer of PAD, creating an interconnect pattern therein, exposing the layer of ARC;

removing the exposed ARC; and

filling the interconnect pattern with a conductive material.

2. The method of claim 1, wherein the conductive material comprises copper.

3. The method of claim 1, wherein the semiconductor surface is a printed circuit board, a flex circuit, a metallized substrate, a glass substrate or a semiconductor device mounting support.

4. The method of claim 1, wherein the semiconductor surface is a semiconductor substrate.

5. The method of claim 4, wherein the semiconductor surface is a ceramic substrate, a glass substrate, a gallium arsenide

substrate, a silicon substrate comprising a single layer of material, such as a silicon wafer or comprising silicon on insulator (SOI) technology and silicon on sapphire (SOS) technology, a doped or undoped semiconductor, an epitaxial layer of silicon supported by a base semiconductor, a sapphire substrate or a substrate used for flat panel displays.

6. The method of claim 1, wherein the layer of Photo-Active Dielectric (PAD) is a polymer.

7. The method of claim 1, wherein the layer of Photo-Active Dielectric (PAD) is a low-k polymer material including polyimides, fluorinated polyimides, polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

8. The method of claim 1, wherein the layer of Photo-Active Dielectric (PAD) is polycarbonate (PC), polystyrene (PS), polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).

9. A method for creation of a dual damascene interconnect pattern, comprising:

providing a layer of conductive material over a semiconductor surface, a layer of Anti Reflective Coating (ARC) having been deposited over the layer of conductive material;

depositing a first layer of Photo-Active Dielectric (PAD) over the layer of ARC;

depositing a second layer of Photo-Active Dielectric over the first layer of Photo-Active Dielectric, the second layer of Photo-Active Dielectric comprising a Photo-Active Dielectric material having a different chemical composition than the first layer of Photo-Active Dielectric;

first patterning and developing the second layer of PAD, creating a trench pattern of a dual damascene pattern therein, exposing the first layer of PAD;

second patterning and developing the exposed first layer of PAD, creating a via pattern of a dual damascene pattern therein aligned with the trench pattern, the second patterning and developing comprising a different type of lithographic exposure than the first patterning and developing, exposing the layer of ARC;

removing the exposed ARC; and

filling the trench pattern and the via pattern with a conductive material.

10. The method of claim 9, wherein the conductive material comprises copper.

11. The method of claim 9, wherein the semiconductor surface is a printed circuit board, a flex circuit, a metallized substrate, a glass substrate or a semiconductor device mounting support.

12. The method of claim 9, wherein the semiconductor surface is a semiconductor substrate.

13. The method of claim 12, wherein the semiconductor surface is a ceramic substrate, a glass substrate, a gallium arsenide substrate, a silicon substrate comprising a single layer of material, such as a silicon wafer or comprising silicon on insulator (SOI) technology and silicon on sapphire (SOS) technology, a doped or undoped semiconductor, an epitaxial layer of silicon supported by a base semiconductor, a sapphire substrate or a substrate used for flat panel displays.

14. The method of claim 9, wherein the first layer of Photo-Active Dielectric (PAD) is a polymer.

15. The method of claim 9, wherein the first layer of Photo-Active Dielectric (PAD) is a low-k polymer material including

polyimides, fluorinated polyimides, polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

16. The method of claim 9, wherein the first layer of Photo-Active Dielectric (PAD) is polycarbonate (PC), polystyrene (PS), polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).

17. The method of claim 9, wherein the second layer of Photo-Active Dielectric (PAD) is a polymer.

18. The method of claim 9, wherein the second layer of Photo-Active Dielectric (PAD) is a low-k polymer material including polyimides, fluorinated polyimides, polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

19. The method of claim 9, wherein the second layer of Photo-Active Dielectric (PAD) is polycarbonate (PC), polystyrene (PS), polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).

20. The method of claim 9, wherein the different type of lithographic exposure is UV lithography, DUV lithography, E-beam lithography, X-ray lithography or ion beam lithography.

21. The method of claim 9, wherein filling the trench pattern and the via pattern with a conductive material comprises methods of metal deposition followed by Chemical Mechanical Polishing (CMP).

22. A method for creation of a dual damascene interconnect pattern, comprising:

providing a layer of conductive material over a semiconductor surface, a first layer of Anti Reflective Coating (ARC) having been deposited over the layer of conductive material;

depositing a first layer of Photo-Active Dielectric (PAD) over the first layer of ARC;

depositing a second layer of ARC over the first layer of PAD;

depositing a second layer of Photo-Active Dielectric over the second layer of ARC, the second layer of Photo-Active Dielectric comprising a Photo-Active Dielectric material having a different chemical composition than the first layer of Photo-Active Dielectric;

first patterning and developing the second layer of PAD, creating an trench pattern of a dual damascene pattern therein, exposing the second layer of ARC;

removing the exposed second layer of ARC, exposing the first layer of PAD;

second patterning and developing the first layer of PAD, creating a via pattern of a dual damascene pattern therein aligned with the trench pattern, the second patterning and developing comprising a different type of lithographic exposure than the first patterning and developing, exposing the first layer of ARC;

removing the exposed first layer of ARC; and

filling the trench pattern and the via pattern with a conductive material.

23. The method of claim 22, wherein the conductive material comprises copper.

24. The method of claim 22, wherein the semiconductor surface is a printed circuit board, a flex circuit, a metallized substrate, a glass substrate or a semiconductor device mounting support.

25. The method of claim 22, wherein the semiconductor surface is a semiconductor substrate.

26. The method of claim 25, wherein the semiconductor surface is a ceramic substrate, a glass substrate, a gallium arsenide substrate, a silicon substrate comprising a single layer of material, such as a silicon wafer or comprising silicon on insulator (SOI) technology and silicon on sapphire (SOS) technology, a doped or undoped semiconductor, an epitaxial layer of silicon supported by a base semiconductor, a sapphire substrate or a substrate used for flat panel displays.

27. The method of claim 22, wherein the first layer of Photo-Active Dielectric (PAD) is a polymer.

28. The method of claim 22, wherein the first layer of Photo-Active Dielectric (PAD) is a low-k polymer material including polyimides, fluorinated polyimides, polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

29. The method of claim 22, wherein the first layer of Photo-Active Dielectric (PAD) is polycarbonate (PC), polystyrene (PS), polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).

30. The method of claim 22, wherein the second layer of Photo-Active Dielectric (PAD) is a polymer.

31. The method of claim 22, wherein the second layer of Photo-Active Dielectric (PAD) is a low-k polymer material including polyimides, fluorinated polyimides, polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

32. The method of claim 22, wherein the second layer of Photo-Active Dielectric (PAD) is polycarbonate (PC), polystyrene (PS), polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).

33. The method of claim 22, wherein the different type of lithographic exposure is UV exposure, DUV exposure, E-beam lithography, X-ray lithography or ion beam lithography.

34. The method of claim 22, wherein filling the trench pattern and the via pattern with a conductive material comprises methods of metal deposition followed by Chemical Mechanical Polishing (CMP).

35. An interconnect pattern created in a layer of insulation material, comprising:

a layer of conductive material provided over a semiconductor surface, a layer of Anti Reflective Coating (ARC) having been deposited over the layer of conductive material;

a layer of Photo-Active Dielectric (PAD) having been deposited over the layer of ARC, the layer of PAD having been patterned and developed, an interconnect pattern having been created therein, the layer of ARC having been removed from underneath the interconnect pattern; and

the interconnect pattern having been filled with a conductive material.

36. The interconnect pattern of claim 35, wherein the conductive material comprises copper.

37. The interconnect pattern of claim 35, wherein the semiconductor surface is a printed circuit board, a flex circuit, a metallized substrate, a glass substrate or a semiconductor device mounting support.

38. The interconnect pattern of claim 35, wherein the semiconductor surface is a semiconductor substrate.

39. The interconnect pattern of claim 38, wherein the semiconductor surface is a ceramic substrate, a glass substrate, a gallium arsenide substrate, a silicon substrate comprising a single layer of material, such as a silicon wafer or comprising silicon on insulator (SOI) technology and silicon on sapphire (SOS) technology, a doped or undoped semiconductor, an epitaxial layer of silicon supported by a base semiconductor, a sapphire substrate or a substrate used for flat panel displays.

40. The interconnect pattern of claim 35, wherein the layer of Photo-Active Dielectric (PAD) is a polymer.

41. The interconnect pattern of claim 35, wherein the layer of Photo-Active Dielectric (PAD) is a low-k polymer material including polyimides, fluorinated polyimides, polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

42. The interconnect pattern of claim 35, wherein the layer of Photo-Active Dielectric (PAD) is polycarbonate (PC), polystyrene (PS), polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).

43. A dual damascene interconnect pattern created in a layer of insulation, comprising:

a layer of conductive material having been provided over a semiconductor surface, a layer of Anti Reflective Coating (ARC) having been deposited over the layer of conductive material;

a first layer of Photo-Active Dielectric (PAD) having been deposited over the layer of ARC, the first layer of PAD having been second patterned and developed, having created a via pattern of a dual damascene pattern therein;

a second layer of Photo-Active Dielectric having been deposited over the first layer of Photo-Active Dielectric, the second layer of Photo-Active Dielectric comprising a Photo-Active Dielectric material having a different chemical composition than the first layer of Photo-Active Dielectric, the second layer of PAD having been first patterned and developed, having created a trench pattern of the dual damascene pattern therein aligned with the via pattern;

the exposed ARC having been removed from underneath the dual damascene interconnect pattern; and

the trench pattern and the via pattern having been filled with a conductive material.

44. The dual damascene interconnect pattern 43, wherein the conductive material comprises copper.

45. The dual damascene interconnect pattern 43, wherein the semiconductor surface is a printed circuit board, a flex circuit, a metallized substrate, a glass substrate or a semiconductor device mounting support.

46. The dual damascene interconnect pattern 43, wherein the semiconductor surface is a semiconductor substrate.

47. The dual damascene interconnect pattern 46, wherein the semiconductor surface is a ceramic substrate, a glass substrate, a gallium arsenide substrate, a silicon substrate comprising a single layer of material, such as a silicon wafer or comprising silicon on insulator (SOI) technology and silicon on sapphire (SOS) technology, a doped or undoped semiconductor, an epitaxial layer of silicon supported by a base semiconductor, a sapphire substrate or a substrate used for flat panel displays.

48. The dual damascene interconnect pattern 43, wherein the first layer of Photo-Active Dielectric (PAD) is a polymer.

49. The dual damascene interconnect pattern 43, wherein the first layer of Photo-Active Dielectric (PAD) is a low-k polymer material including polyimides, fluorinated polyimides,

polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

50. The dual damascene interconnect pattern 43, wherein the first layer of Photo-Active Dielectric (PAD) is polycarbonate (PC), polystyrene (PS), polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).

51. The dual damascene interconnect pattern 43, wherein the second layer of Photo-Active Dielectric (PAD) is a polymer.

52. The dual damascene interconnect pattern 43, wherein the second layer of Photo-Active Dielectric (PAD) is a low-k polymer material including polyimides, fluorinated polyimides, polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

53. The dual damascene interconnect pattern 43, wherein the second layer of Photo-Active Dielectric (PAD) is polycarbonate (PC), polystyrene (PS), polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).

54. A dual damascene interconnect pattern formed in a layer of insulating material, comprising:

a layer of conductive material having been provided over a semiconductor surface, a first layer of Anti Reflective Coating (ARC) having been deposited over the layer of conductive material;

a first layer of Photo-Active Dielectric (PAD) having been deposited over the first layer of ARC, the first layer of PAD having been second patterned and developed, having created a via pattern of a dual damascene pattern;

a second layer of ARC having been deposited over the first layer of PAD;

a second layer of Photo-Active Dielectric having been deposited over the second layer of ARC, the second layer of Photo-Active Dielectric comprising a Photo-Active Dielectric material having a different chemical composition than the first layer of Photo-Active Dielectric, the second layer of PAD having been patterned and developed, having created a trench pattern of a dual damascene pattern therein aligned with the via pattern;

the second layer of ARC having been removed from underneath the trench pattern;

the first layer of ARC having been removed from underneath the via pattern; and

the trench pattern and the via pattern having been filled with a conductive material.

55. The dual damascene interconnect pattern of claim 54, wherein the conductive material is copper.

56. The dual damascene interconnect pattern of claim 54, wherein the semiconductor surface is a printed circuit board, a flex circuit, a metallized substrate, a glass substrate or a semiconductor device mounting support.

57. The dual damascene interconnect pattern of claim 54, wherein the semiconductor surface is a semiconductor substrate.

58. The dual damascene interconnect pattern of claim 57, wherein the semiconductor surface is a ceramic substrate, a glass substrate, a gallium arsenide substrate, a silicon substrate comprising a single layer of material, such as a silicon wafer or comprising silicon on insulator (SOI) technology and silicon on sapphire (SOS) technology, a doped or undoped semiconductor, an epitaxial layer of silicon supported by a base semiconductor, a sapphire substrate or a substrate used for flat panel displays.

59. The dual damascene interconnect pattern of claim 54, wherein the first layer of Photo-Active Dielectric (PAD) is a polymer.

60. The dual damascene interconnect pattern of claim 54, wherein the first layer of Photo-Active Dielectric (PAD) is a low-k polymer material including polyimides, fluorinated polyimides, polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

61. The dual damascene interconnect pattern of claim 54, wherein the first layer of Photo-Active Dielectric (PAD) is polycarbonate (PC), polystyrene (PS), polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).

62. The dual damascene interconnect pattern of claim 54, wherein the second layer of Photo-Active Dielectric (PAD) is a polymer.

63. The dual damascene interconnect pattern of claim 54, wherein the second layer of Photo-Active Dielectric (PAD) is a low-k polymer material including polyimides, fluorinated polyimides, polysilsequioxane, benzocyclobutene (BCB), parlene F, parlene N and amorphous polytetrafluorothylene.

64. The dual damascene interconnect pattern of claim 54, wherein the second layer of Photo-Active Dielectric (PAD) is polycarbonate (PC), polystyrene (PS), polyoxides (PO), polymethylmethacrylate (PPMA) and poly-polyoxides (PPO).